10/12/2010 IRIS FAQ Addendum

Q: Can you please clarify if a team of proposers from multiple universities need to submit one proposal abstract by the lead institution or if each investigator from each institution needs to submit a proposal abstract?
A: The lead institution is expected to submit one proposal for the entire team.

Q: Is DARPA anticipating participation from universities given the classified nature of Phase II?
A: The BAA and IRIS program are structured in such a way that universities may participate; Phase I-only proposals may be accepted as well.

Q: For Technical Area 1B, in what format is the low-level netlist?
A: It will be a transistor-level netlist.

Q: Will a data-sheet with details regarding pin-out locations, power, timing, etc. be provided?
A: Yes, a data-sheet will be provided.

Q: Will a 45 nm process design kit (PDK) be provided?
A: As long as the appropriate licensing agreements are in place, a 45 nm PDK may be obtained from a number of sources.

Q: Will the integrated circuit test chips used in Technical Area 1A have the same underlying design as the netlist test article provided for Technical Area 1B?
A: No.

Q: Will the 10 test devices provided as GFE be identical (within manufacturing variances)?
A: For Technical Area 4, the 10 government-provided test articles are expected to be identical within manufacturing tolerances.

Q: Is x-ray imaging consistent with the non-destructive goal of IRIS, specifically with regards to Technical Areas 1 and 2?
A: In order for a technique to qualify as non-destructive, the device must retain all pre-evaluation functionality after testing.

Q: On page 39 of BAA-10-33, the abstract submission date is listed as Friday, October 14, 2010. Is the submission date Thursday, October 14, 2010, or Friday, October 15, 2010?
A: The abstract submission date is Thursday, October 14, 2010.

IRIS BAA FAQ

Q: Does the information entropy technique or definition apply in the mixed-signal domain, or is it specific to the digital domain?

A: "Information Entropy" or "Shannon Entropy", as discussed at the IRIS Industry Day, was suggested as a useful means of quantifying the total potential amount of information contained in a logic block. In the digital example we shared, information entropy H(S) was associated with the probability (hence predictability) of any one binary output word appearing as the result of an arbitrarily complex Boolean operation. A device which outputs analog information, on the other hand, has the ability to express a continuous range of output data for each channel. In this scenario, an analog transfer function determines the output, and our perception of functional complexity is associated with our ability to de-convolve analog function rather than Boolean operation. The mathematics for this approach is described in the Kullback-Leibler divergence theorem.

Submitted Questions

Q: Can you delay the abstract and full proposal response dates?
A: The abstract submission date has been pushed to Thursday October 14, 2010 at 4:00 pm EDT. The full proposal date has been pushed to Tuesday December 7, 2010 at 4:00 pm EST.

Q: Must proposers provide a detailed budget for Phase I and II?
A: Full and detailed budgets must be provided for both Phases.

Q: What level of functionality is in-scope for IRIS? FPU-level or adder-level?
A: All levels above the standard cell level and below the core level are of interest to DARPA.

Q: Are performers permitted to use only specified test vectors, or may further test vectors be applied?
A: Yes; further test vectors may be applied.

Q: Are the 10 parts in Technical Area 4 still expected to be useful after testing?
A: No, just screen batch.

Q: Is reactive etch the preferred method or does DARPA allow for other reverse engineering approaches?
A: DARPA has no preference.

Q: Is DARPA interested in functions that could result from multiple core functions working as an ensemble, i.e. distributed aggregate functions?
A: Yes

Q: Is DARPA interested in functions beyond standard unit cell functions, i.e. ‘unknown unknowns’?

A: Yes

Q: Can tests in Technical Area 4 be destructive tests?
A: Yes

Q: Will additional test articles be available in Technical Area 4 if destructive tests are first used to develop a capability?
A: Only 10 official test articles will be provided by DARPA; development work should be performed on your own test articles.

Q: Will testing be performed at wafer or die level for Technical Area 4?
A: The plan for Technical Area 4 is that testing of the government-provided test articles will be performed at the packaged die level.

Q: What will be the approximate design lifetime of the test articles for Technical Area 4?
A: The lifetimes of the test articles will be consistent with that of typical CMOS commercial parts fabricated in the 90 and 45 nm nodes for Technical Area 4A and in the 130 and 90 nm nodes for Technical Area 4B.

Q: Will the Government team be using accelerated lifetime testing to determine baseline reliability?
A: Yes

Q: Will the test articles in Technical Area 1B be in GDSII format, flattened verilog or other?
A: Both GDSII and verilog will be made available.

Q: Will the test articles in Technical Area 1A contain scan chains?
A: Potentially

Q: Will there be additional test articles be made available at the beginning of each phase for technique development purposes?
A: The government will only provide evaluation test articles.

Q: Should the extracted flattened netlist in Technical Area 1A be at the transistor level or at the gate level?
A: Either

Q: Will the Technical Areas' 2 & 4 test article form factors (pin count, package outline, etc.) be provided in advance to facilitate test fixtures?
A: Yes

Q: Will the government test articles from Technical Areas 1, 2, & 4 be delivered packaged with evaluation boards or other test/characterization boards?
A: The government will deliver articles with evaluation boards.

Q: Is 3rd Party IP which potentially impacts the reliability of the part considered in-scope?
A: Yes

Q: Can you elaborate on the type of specifications that will be provided in Technical Area 3?
A: The specifications will be consistent with what can be expected from commercial 3rd Party IP vendors.

Q: What is the form of the Soft IP test article for Technical Area 3A?
A: The Soft IP test article will be in the form of synthesizable code that can be inserted into a design.

Q: Will the soft IP test article for Technical Area 3A be obfuscated?
A: No

Q: What is the test article answer format expected from performers?
A: Please include in your proposal how you plan to provide answers.

Q: Can you define abstract functions in a countable way?
A: Please provide recommendations in your proposal.

Q: For Technical Area 4, should a performer assume that a malicious modification has been made to the IC that potentially affects reliability?
A: Only the test articles in Phase II of Technical Area 4 will contain malicious modifications that may affect reliability.

Q: For Technical Area 3B, should performers consider reconfiguration effects?
A: Yes

Q: Will you specify the target device for technical area 3B?
A: FPGA IP will be available for both the Xilinx Virtex family and for the Altera Stratix family.

Q: For Technical Area 3A, will the Soft IP be synthesizable? What ASIC/FPGA tools will the scripts target?
A: Customizable synthesis scripts will be provided with the Soft IP test article.

Q: Can we team with other performers after feedback is returned from the abstract phase?
A: Yes; the content of your abstract is not binding with respect to your final proposal.

Q: In the case of a university proposing fundamental research, can you comment on the choice between teaming with a company or submitting a proposal in conjunction with another company or organization?
A: We cannot comment on teaming arrangements.

Q: Is TFIMS available for abstract submissions?

A: Yes

Q: Is TFIMS the preferred method for submissions?
A: TFIMS is the required method for submission of all proposals except those requesting an assistance instrument (grant or cooperative agreement). Submission of proposals requesting award of an assistance instrument must be submitted either electronically via grants.gov or in hardcopy.

Q: Will DARPA sponsor clearances for Phase 2 performers?
A: DARPA cannot sponsor SECRET-level clearances for non-government organizations; however, cleared prime contractors may sponsor SECRET-level clearances for non-cleared subcontractors.

Q: Will there be multiple awards within a single technical area?
A: Yes

Q: Are we receiving marketing literature or a data sheet with block diagrams?
A: You will receive both.

Q: Do you have an expected funding profile?
A: No

Q: Will performers receive a netlist to derive the functionality?
A: Yes, for Technical Area 1B

Q: What is the form or package in which the chips will be provided?
A: For Technical Area 1A, the chips will be packaged or unpackaged.

Q: Must the reliability screening of devices for Technical Area 4 include all three categories of reliability: intrinsic, manufacturing defects and soft-errors?
A: No; the primary focus of Technical Area 4 is on intrinsic reliability.

Q: What constraints can be assumed for the reliability test, e.g. max/min temperature, max/min Vdd, max/min Idd, etc.?
A: There are no constraints.

Q: In Technical Area 4, what information will or will not be included as ‘detailed information’ on planned test articles?
A: Please provide recommendations in your proposal.

Q: What kinds of test patterns will performers receive? Functional test patterns or ATPG test patterns?
A: Performers will be provided primarily functional test patterns.

Q: Are design techniques allowed to be developed in Technical Area 4?
A: Yes

Q: Are you able to provide a physical size or rough estimate of the # of gates for the test articles in Technical Areas 1 and 2?
A: The sizes of the test articles will be consistent with the sizes of commercially available mixed-signal and digital designs.

Q: In Technical Area 1, are non-destructive techniques that potentially reduce the reliability of the chip in-scope?
A: Yes

Q: Are techniques in which a circuit (such as a health-monitoring circuit) is included in the IC in-scope for IRIS?
A: This approach does not apply to any of the published tech areas; please submit ideas in this area to the open office BAA instead of the IRIS BAA.

Q: If a proposer has unrelated solutions to unrelated thrusts, are you expecting a single or multiple abstracts?
A: A single abstract is expected.

Q: Must all of Phase I be unclassified?
A: Yes

Q: Can you further specify the difference between non-destructive and destructive testing?
A: After non-destructive testing, the chip must retain all pre-testing functionality.

Q: Will the names of the government test team be announced?
A: Not publicly

Q: Should performers trust the tools that provide the evaluations, and should the performers trust that the specification is accurate?
A: The data provided for the test should be assumed to be accurate.

Q: Are the specifications assumed to be English language or C-models?
A: The government will distribute English language specifications for the test articles. There will be no C-models provided.

Q: What is the abstract page limit?
A: Please follow the guidelines for abstract submission outlined on page 33 of the BAA. Fifteen pages maximum may be submitted for an abstract. The abstract format, but not necessarily the abstract page count, is expected to follow the guidelines listed in the Full Proposal Format for Volumes I and II.